Claims

[c1] An integrated circuit comprising:
a standard dimension carrier substrate;
an information router integrated on the carrier substrate; and
system memory also integrated on the carrier substrate and in electrical communication with the information router via at least one of a plurality of electrical leads associated with the carrier substrate, wherein system instructions may be stored and retrieved from the system memory through the information router.

[c2] The integrated circuit of claim 1 wherein the information router is disposed within an application specific integrated circuit die.

[c3] The integrated circuit of claim 2 further comprising:
a graphics controller further disposed within the application specific integrated circuit die in conjunction with the information router.

[c4] The integrated circuit of claim 3 further comprising:
graphics memory also integrated on the carrier substrate and in electrical communication with the graphics controller via at least one of the plurality of electrical leads associated with the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory.

[c5] The integrated circuit of claim 2 wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds.

[c6] The integrated circuit of claim 2 wherein the system memory is disposed on a top surface of the carrier substrate and the application specific integrated circuit die is coupled to a bottom surface of the carrier substrate of the packaged chip using a flip chip technology.

[c7] The integrated circuit of claim 1 wherein the system memory is disposed within a chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

[c8] The integrated circuit of claim 1 wherein the system memory is a memory die coupled to the carrier substrate using a plurality of wirebonds.

[c9] The integrated circuit of claim 1 wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

[c10] An integrated circuit comprising:
a standard dimension carrier substrate having a plurality of electrical leads disposed between a top surface and a bottom surface of the carrier substrate;
an application specific integrated circuit die coupled to the bottom surface of the carrier substrate, wherein the application specific integrated circuit die includes a north bridge; and
system memory integrated on the top surface of the carrier substrate and in electrical communication with the north bridge via at least one of the plurality of electrical leads within the carrier substrate, wherein system instructions may be stored and retrieved from the system memory through the north bridge, within the packaged chip.

[c11] The integrated circuit of claim 10 wherein the application specific integrated circuit die further includes a graphics controller in conjunction with the north bridge.

[c12] The integrated circuit of claim 11 further comprising:
graphics memory also integrated on the carrier substrate and in electrical communication with the graphics processor via at least one of the plurality of electrical leads within the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory, within the packaged chip.

[c13] The integrated circuit of claim 10 wherein the application specific integrated circuit die is coupled to the bottom surface of the carrier substrate using a plurality of wirebonds.

[c14] The integrated circuit of claim 10 wherein the system memory is disposed within at least one chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

[c15] The integrated circuit of claim 10 wherein the system memory is at least one memory die coupled to the carrier substrate using a plurality of wirebonds.

[c16] The integrated circuit of claim 10 wherein the north bridge within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

[c17] A method for making an integrated circuit comprising:
coupling a system memory to a top surface of a standard dimension carrier substrate having a plurality of wires disposed within a carrier substrate, the method of the carrier substrate; and
coupling a north bridge to a bottom surface of the carrier substrate wherein the system memory may receive and transmit system instructions through the north bridge via the plurality of internal wirings within the carrier substrate.

[c18] The method of claim 17 wherein when the system memory is composed of a chip scale package memory having a plurality of contact pins, the step of coupling the system memory to the top surface of the carrier substrate includes soldering the plurality of contact pins to a first plurality of the internal wirings within the carrier substrate and when the system memory is composed of at least one memory die, the step of coupling the system memory on the top surface of the carrier substrate includes wirebonding the at least one memory die to a second plurality of the internal wirings.

[c19] The method of claim 17 wherein the north bridge is disposed within an application specific integrated circuit and the step of coupling the north bridge on the bottom surface of the carrier substrate includes wirebonding the application specific integrated circuit die to a plurality of the internal wirings.

[c20] The method of claim 18 wherein the application specific integrated circuit die further includes a graphics processor in conjunction with the north bridge.